1. (Once Amended) An integrated circuit inductor comprising:

a substrate;

a spiral inductor metalization pattern disposed on the substrate including a plurality of parallel tracks in a spiral pattern each track having a first end and a second end and having the first ends coupled together and the second ends coupled together; and

a n+ diffusion layer disposed in the substrate beneath the spiral inductor metalization pattern.

5. (Once Amended) The integrated circuit inductor of claim 1, in which the plurality of tracks are disposed in a common layer of the substrate.

6. (Once Amended) The integrated circuit inductor of claim 1, in which the plurality of tracks are disposed in different layers of the substrate.

7. (Once Amended) The integrated circuit inductor of claim 1, in which the plurality of tracks are disposed in different layers of the substrate and coupled together with a via.

10. (Once Amended) The integrated circuit inductor of claim 1, in which the n^+ diffusion layer is formed in a fingered pattern from n+ material having n+ fingers electrically isolated by regions of polysilicon to produce the fingered pattern.

11.(Once Amended) The integrated circuit inductor of claim 10, in which the fingered pattern is coupled to a common ground reference.

12.(Once Amended) The integrated circuit inductor of claim 10, in which the n^+ diffusion layer further comprises a second fingered pattern coupled to the common ground reference by a conductive strip that does not provide a ground loop path.

14. (Once Amended) An integrated circuit inductor comprising:

a substrate having a first layer and a second layer;

a first track disposed on the first layer in a first spiral pattern;

a second track disposed on the second layer in a second spiral pattern and oriented parallel to the first spiral pattern; and

a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track.

15. (Once Amended) An integrated inductor comprising:

a substrate having a first layer and a second layer;

a first outer transmission line disposed on the first layer in a spiral pattern;

a second inner transmission line disposed on the first layer in a spiral pattern such that the second inner transmission line is loosely coupled to the first outer transmission line;

a first transmission line first end of the first outer transmission line directly coupled to a second transmission line first end of the second inner transmission line, and a first transmission line second end of the first outer transmission line directly coupled to a second transmission line second end of the second inner transmission line;

a third outer transmission line disposed on the second layer in a spiral pattern and aligned above the first transmission line and directly coupled to the first transmission line;

a fourth inner transmission line disposed on the substrate's second layer in a spiral pattern such that the fourth inner transmission line is coupled to the first transmission line and aligned above the second transmission line and directly coupled to the second transmission line; and

the first transmission line first end and the second transmission line first end forming an input for the integrated inductor, the first transmission line second end and the second transmission line second end forming an output for the integrated inductor.

Please add the following new claims 24-28:

24. An integrated circuit inductor, comprising:

a substrate having a first layer and a second layer;

a first spiral pattern disposed on the first layer of the substrate and having a first end and a second end;

a second spiral pattern disposed on the second layer of the substrate and oriented parallel to the first spiral pattern, and having a first end and a second end; and

the first end of the a first spiral pattern connected to the first end of the second spiral pattern and forming an input for the integrated circuit inductor, and the second end of the first spiral pattern connected to the second end of the second spiral pattern and forming an output for the integrated circuit inductor.

25. The integrated circuit inductor of claim 24, further comprising a plurality of via holes disposed along a length of the first spiral pattern and connected to the second spiral pattern.

26. The integrated circuit inductor of claim 24, further comprising a n+ diffusion layer disposed in the substrate beneath the first spiral pattern and the second spiral pattern.

27. The integrated circuit inductor of claim 26, wherein the n^+ diffusion layer is formed in a fingered pattern from n+ material having n+ fingers electrically isolated by regions of polysilicon to produce the fingered pattern.

28. The integrated inductor of claim 24, wherein the substrate is a CMOS substrate.